The Specification

Please amend the Title on Pages 1 and 47 of the Specification as follows:

COUPLING PROCESSORS TO EACH OTHER FOR HIGH PERFORMANCE COMPUTING ~~SYSTEM AND METHOD~~ (HPC)

Please amend the Paragraph starting at Line 21 of Page 12 as follows:

In general, disk farm 140 is any memory, database or storage area network (SAN) for storing jobs 150, profiles, boot images, or other HPC information. According to the illustrated embodiment, disk farm 140 includes one or more storage clients 142. ~~Disk farm 140 may process and route data packets according to any of a number of communication protocols, for example, Infiniband (IB), Gigabit Ethernet (GE), or FibreChannel (FC).~~ Disk farm 140 may process and route data packets according to any of a number of communication protocols, for example, INFINIBAND (IB), Gigabit Ethernet (GE), or FibreChannel (FC). Data packets are typically used to transport data within disk farm 140. A data packet may include a header that has a source identifier and a destination identifier. The source identifier, for example, a source address, identifies the transmitter of information, and the destination identifier, for example, a destination address, identifies the recipient of the information.

Please amend the Paragraph starting at Line 21 of Page 18 as follows:

Blade 315 is an integrated fabric architecture that distributes the fabric switching components uniformly across nodes 115 in grid 110, thereby possibly reducing or eliminating any centralized switching function, increasing the fault tolerance, and allowing message passing in parallel. More specifically, blade 315 includes an integrated switch 345. Switch 345 includes any number of ports that may allow for different topologies. For example, switch 345 may be an eight-port switch that enables a tighter three-dimensional mesh or 3D

Torus topology. These eight ports include two "X" connections for linking to neighbor nodes 115 along an X-axis, two "Y" connections for linking to neighbor nodes 115 along a Y-axis, two "Z" connections for linking to neighbor nodes 115 along a Z-axis, and two connections for linking to management node 105. ~~In one embodiment, switch 345 may be a standard eight port Infiniband 4x switch IC, thereby easily providing built in fabric switching.~~ In one embodiment, switch 345 may be a standard eight port INFINIBAND-4x switch IC, thereby easily providing built-in fabric switching. Switch 345 may also comprise a twenty-four port switch that allows for multidimensional topologies, such a 4-D Torus, or other non-traditional topologies of greater than three dimensions. Moreover, nodes 115 may further interconnected along a diagonal axis, thereby reducing jumps or hops of communications between relatively distant nodes 115. For example, a first node 115 may be connected with a second node 115 that physically resides along a northeasterly axis several three dimensional "jumps" away.

Please amend the Paragraph starting at Line 8 of Page 21 as follows:

~~FIGURE 3B illustrates a blade 315 that includes two processors 320a and 320b, memory 340, HyperTransport/ peripheral component interconnect (HT/PCI) bridges 330a and 330b, and two HCAs 335a and 335b.~~ FIGURE 3B illustrates a blade 315 that includes two processors 320a and 320b, memory 340, HYPERTRANSPORT / peripheral component interconnect (HT/PCI) bridges 330a and 330b, and two HCAs 335a and 335b.

Please amend the Paragraph starting at Line 12 of Page 21 as follows:

Example blade 315 includes at least two processors 320. Processor 320 executes instructions and manipulates data to perform the operations of blade 315 such as, for example, a central processing unit (CPU). In the illustrated embodiment, processor 320 may comprise an Opteron processor or other similar processor or derivative. In this embodiment, the Opteron processor design supports the development of a well balanced building block for

grid 110. Regardless, the dual processor module may provide four to five Gigaflop usable performance and the next generation technology helps solve memory bandwidth limitation. But blade 315 may more than two processors 320 without departing from the scope of this disclosure. Accordingly, processor 320 has efficient memory bandwidth and, typically, has the memory controller built into the processor chip. ~~In this embodiment, each processor 320 has one or more HyperTransport™ (or other similar conduit type) links 325.~~ In this embodiment, each processor 320 has one or more HYPERTRANSPORT (or other similar conduit type) links 325.

Please amend the Paragraph starting at Line 1 of Page 22 as follows:

Generally, HT link 325 comprises any high-speed, low latency link designed to increase the communication speed between integrated components. This helps reduce the number of buses in blade 315, which can reduce system bottlenecks. HT link 325 supports processor to processor communications for cache coherent multiprocessor blades 315. Using HT links 325, up to eight processors 320 may be placed on blade 315. ~~If utilized, HyperTransport may provide bandwidth of 6.4 GB/sec, 12.8, or more, thereby providing a better than forty-fold increase in data throughput over legacy PCI buses. Further HyperTransport technology may be compatible with legacy I/O standards, such as PCI, and other technologies, such as PCI-X.~~ If utilized, HYPERTRANSPORT may provide bandwidth of 6.4 GB/sec, 12.8, or more, thereby providing a better than forty-fold increase in data throughput over legacy PCI buses. Further HYPERTRANSPORT technology may be compatible with legacy I/O standards, such as PCI, and other technologies, such as PCI-X.

Please amend the Paragraph starting at Line 14 of Page 22 as follows:

Blade 315 further includes HT/PCI bridge 330 and HCA 335. PCI bridge 330 may be designed in compliance with PCI Local Bus Specification Revision 2.2 or 3.0 or PCI Express Base Specification 1.0a or any derivatives thereof. HCA 335 comprises any component

providing channel-based I/O within server 102. ~~In one embodiment, HCA 335 comprises an Infiniband HCA. Infiniband channels are typically created by attaching host channel adapters and target channel adapters, which enable remote storage and network connectivity into an Infiniband fabric, illustrated in more detail in FIGURE 3B. HyperTransport 325 to PCI-Express Bridge 330 and HCA 335 may create a full-duplex 2GB/sec I/O channel for each processor 320.~~ In one embodiment, HCA 335 comprises an INFINIBAND HCA. INFINIBAND channels are typically created by attaching host channel adapters and target channel adapters, which enable remote storage and network connectivity into an INFINIBAND fabric, illustrated in more detail in FIGURE 3B. HYPERTRANSPORT 325 to PCI-Express Bridge 330 and HCA 335 may create a full-duplex 2GB/sec I/O channel for each processor 320. In certain embodiments, this provides sufficient bandwidth to support processor-processor communications in distributed HPC environment 100. Further, this provides blade 315 with I/O performance nearly or substantially balanced with the performance of processors 320.